

Figure 1

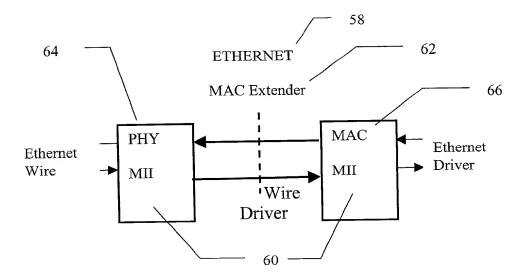


Figure 2

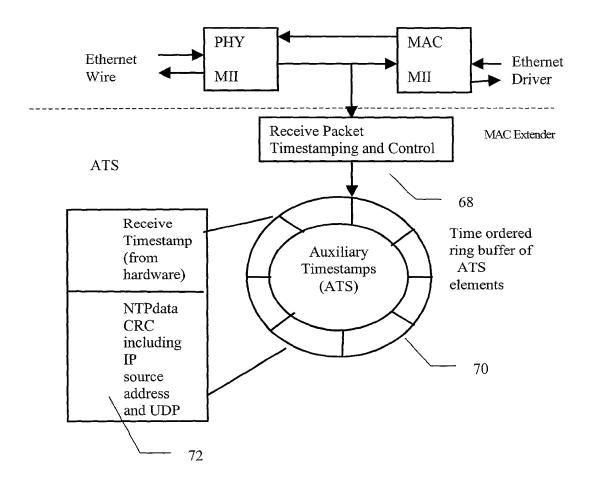


Figure 3

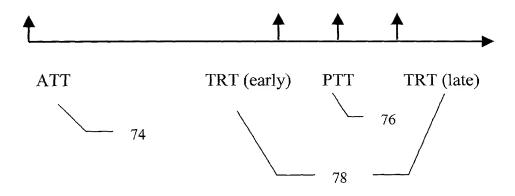


Figure 4

Block Diagram of "Joplin" Card - Full Intercept Version 66 Ref. 1 PPS and 10 MHz Test Switches 62 64 Modular 8 pin (RJ-45 style) CPU Xilınx PHY PLL in Support MII Rx Circuits MAC MII (MAC (JTAG, RAM, ROM, FLASH, CNTL Tx Magnetics CNTL Extender) etc) (4x Mult) Filter & Connector RS/232 Clock (Ref. Time) May be integrated Test Point Osc Array Logger DAC 25 MHz 25 MHz DE-9 (x2) +3 3 V Power **→** +5 V 5 V ín Conditioning -Power Distribution → +12 V

Figure 5

& Regulation

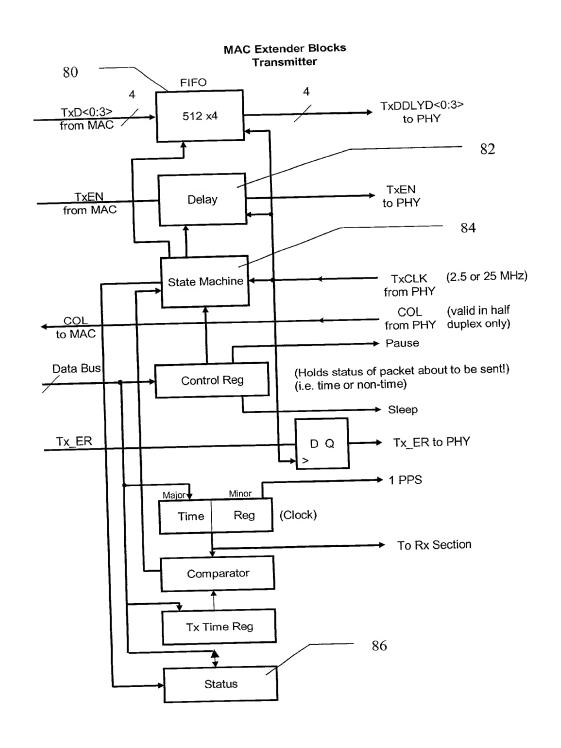


Figure 6

MAC Extender Receiver

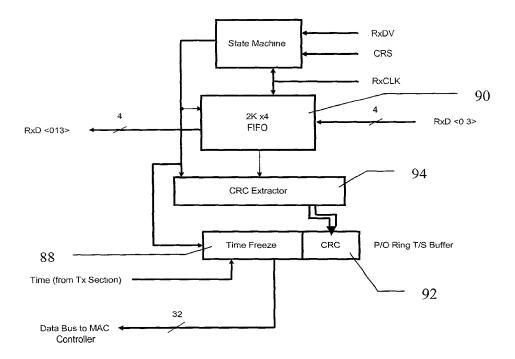


Figure 7

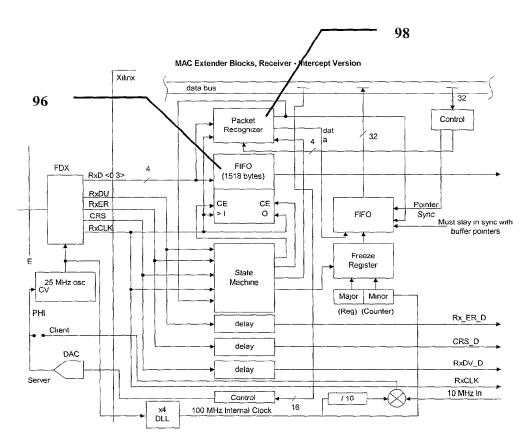


Figure 8

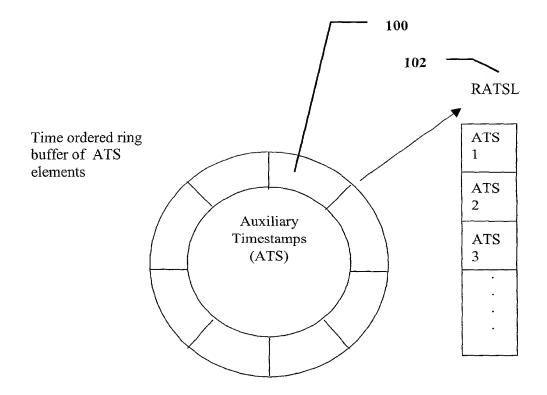


Figure 9

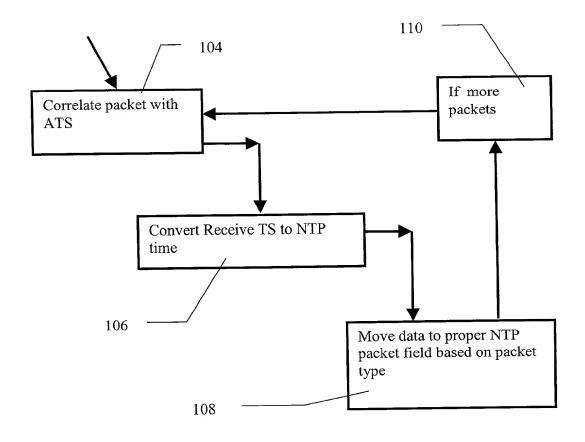


Figure 10

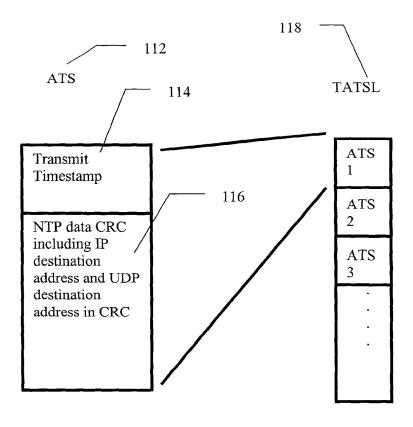


Figure 11

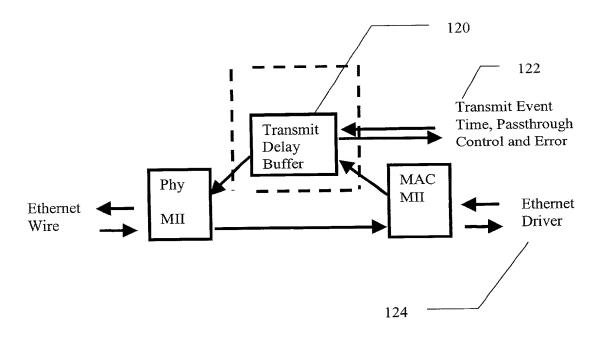


Figure 12

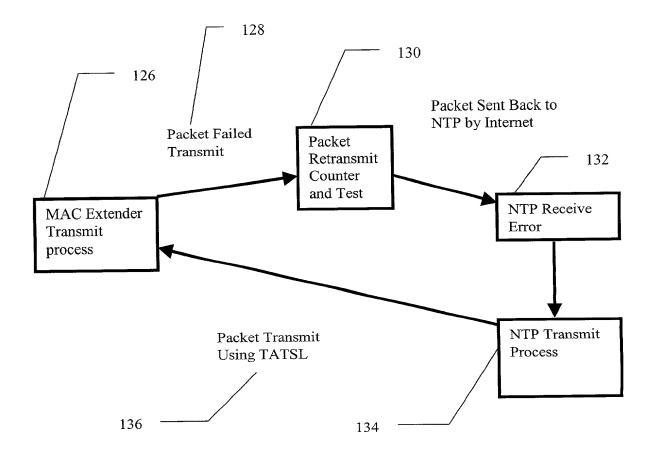


Figure 13

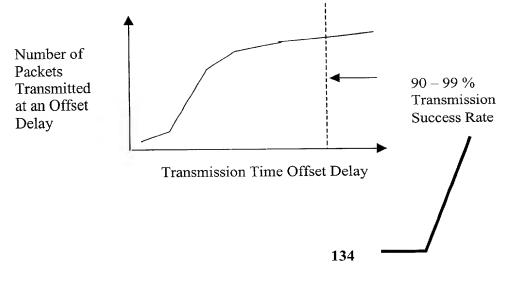


Figure 14

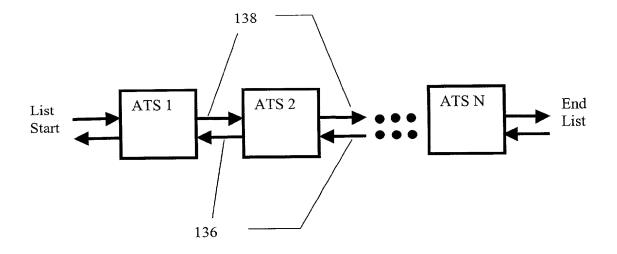


Figure 15

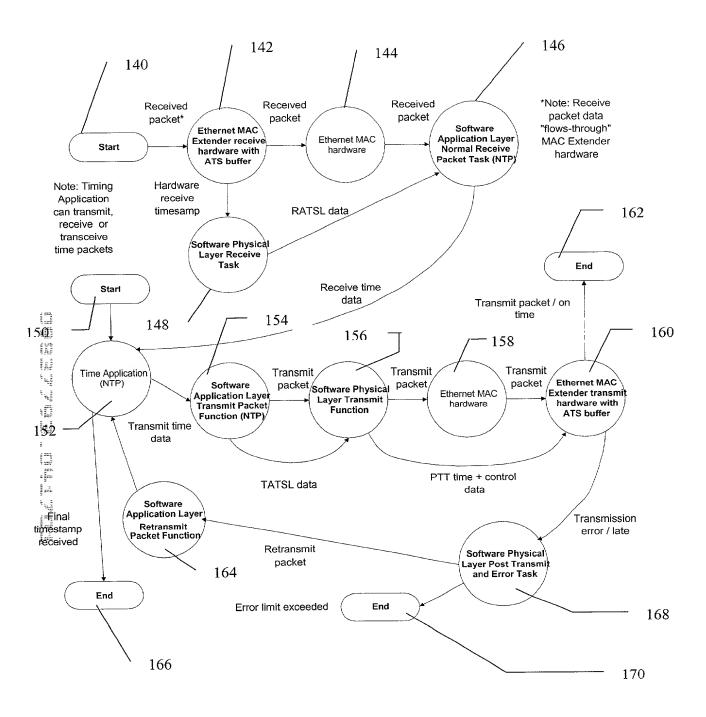


Figure 16

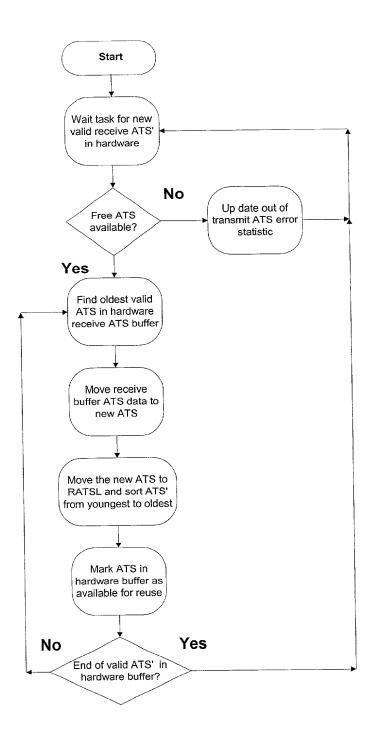


Figure 17

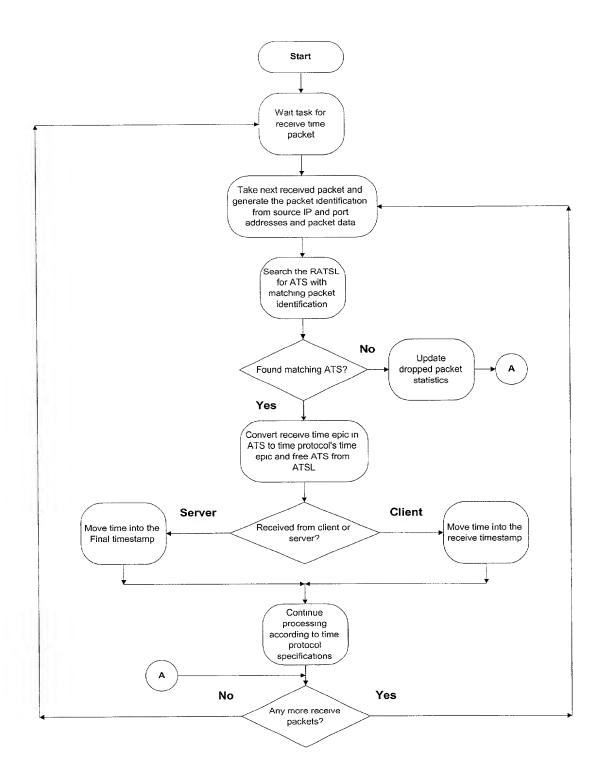


Figure 18

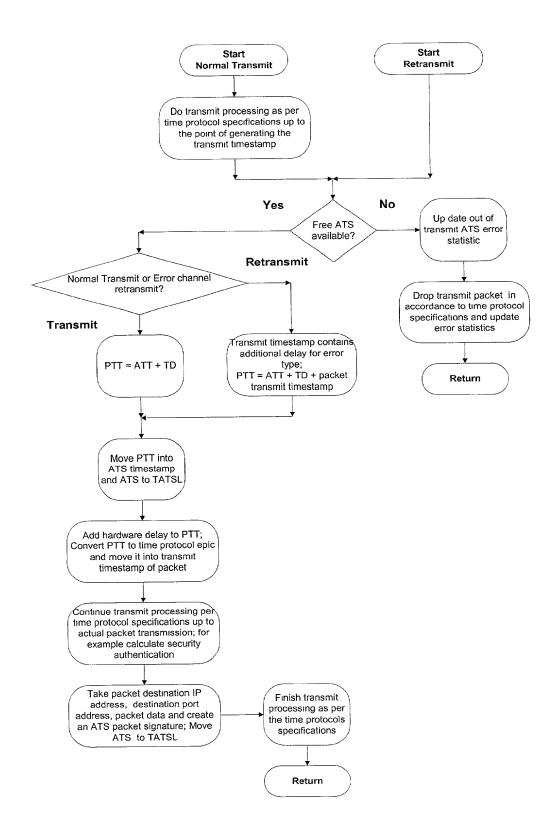


Figure 19

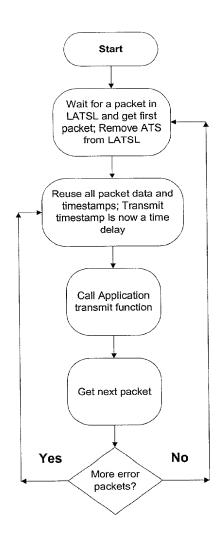


Figure 20

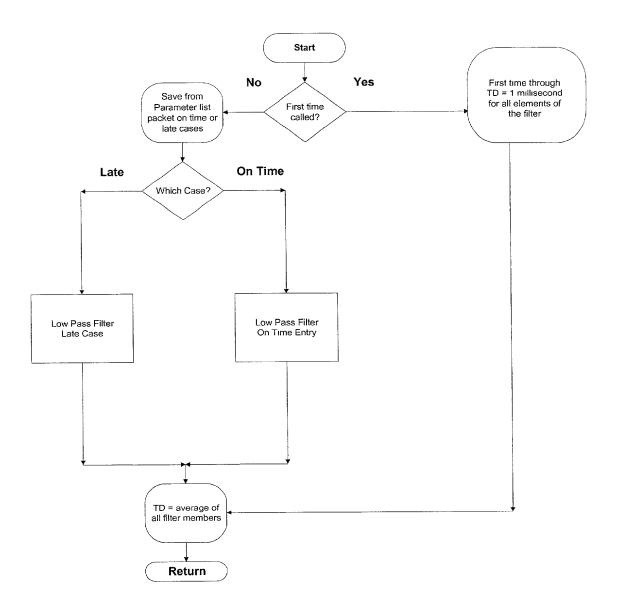


Figure 21

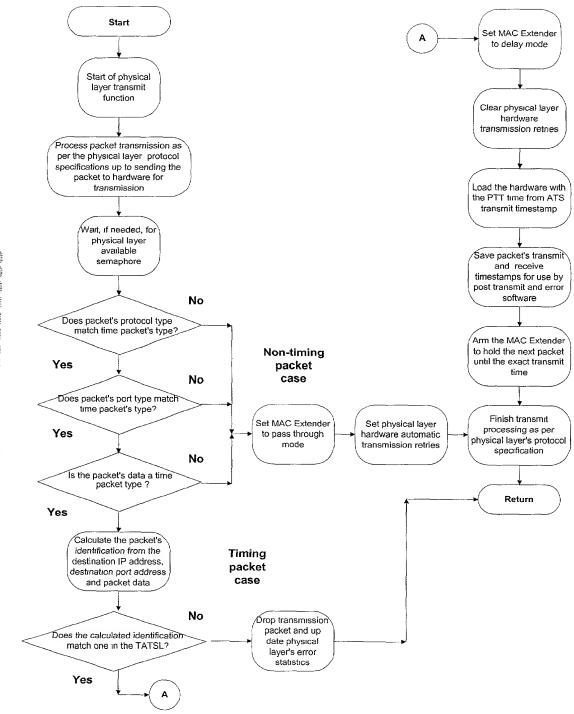


Figure 22

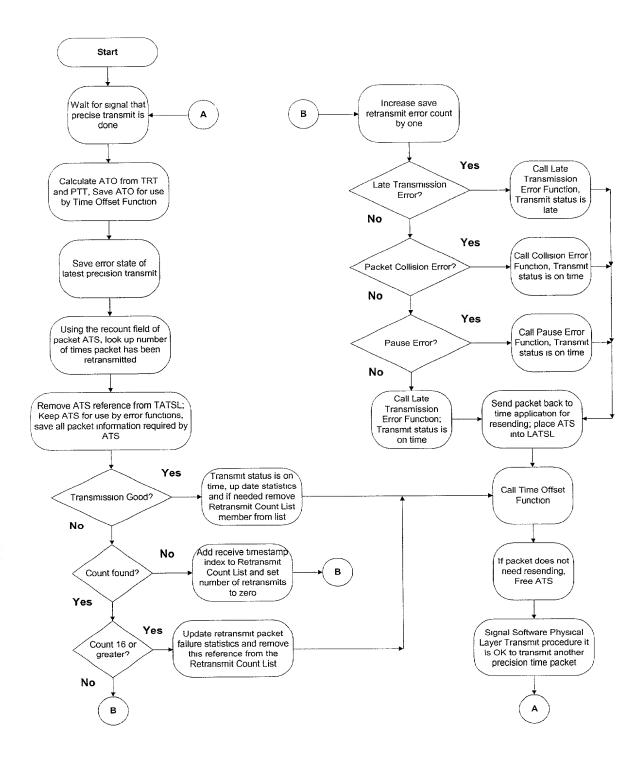


Figure 23

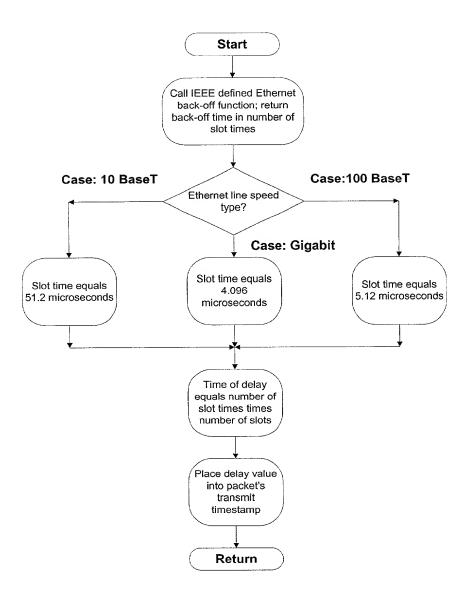


Figure 24

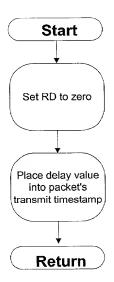


Figure 25

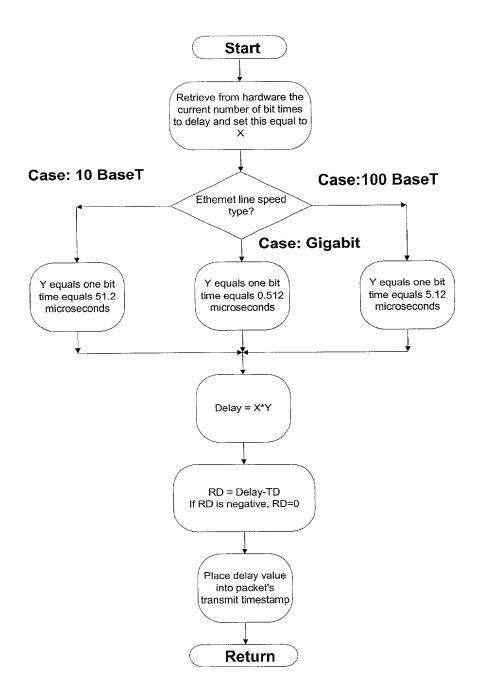


Figure 26

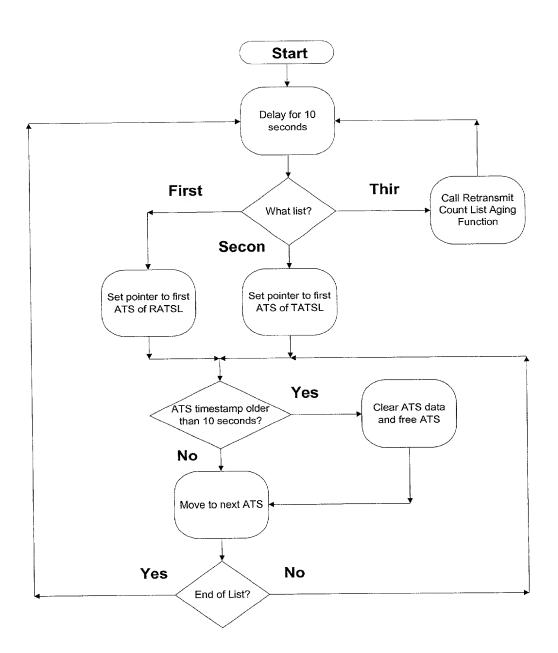


Figure 27

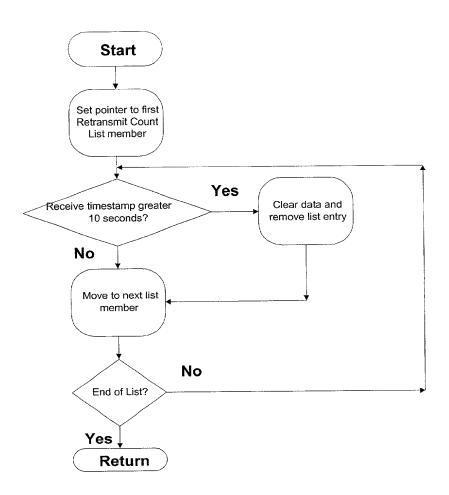


Figure 28